Twin NAND Device Structure, Array Operations and Fabrication Method

This application claims priority to Provisional Patent Application serial number 60/311,879, filed on August 13, 2001, which is herein incorporated by reference

<This application is a DIV of 10/218,210 filed 8/13/02, PAT. 6,670,240>

BACKGROUND OF THE INVENTION

1. Field of Invention.

The present invention is related to semiconductor memory and more particular non-volatile NAND memory arrays.

2. Description of related art.

In F. Masuoka et al., "A New NAND Cell for Ultra High Density 5V-only EEPROMs" , May 1988, Proc 1988 Symposium on VLSI Technology, IV-5 pp33-34) a floating gate NAND cell, shown in FIG. 1A of prior art, is described that has been used widely as Non-volatile memory. Since the memory cell is placed in series without any contact, the density is very high even though the process complexity is high and the read current level is very small. The storage element in the flash NAND is a polysilicon floating gate 200 residing under a word line 201 in the example shown in FIG 1A. The floating gate can be replaced by a nitride layer sandwiched between bottom and top oxide layers (Oxide-Nitride-Oxide) 202 laying under a word gate 201 as shown in the example in FIG. 1B and FIG. 1C of prior art. The ONO layer sandwich stores electron or hole charges in the nitride or interface trap sites as suggested in Y. Hayashi et al. "Nonvolatile Semiconductor memory and its Programming Method", JP 11-22940, 12/05/1997. This ONO storage approach for the MONOS NAND simplifies the process